CHARACTERIZATION AND MODELING OF HOT CARRIER DEGRADATION IN SILICON-GERMANIUM HBTS

A Thesis
Presented to
The Academic Faculty

by

Brian R Wier

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2015

CHARACTERIZATION AND MODELING OF HOT CARRIER DEGRADATION IN SILICON-GERMANIUM HBTS

Approved by:

Professor John D. Cressler, Advisor
Department of Electrical and Computer Engineering
Georgia Institute of Technology

Professor John Papapolymerou
Department of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Douglas Yoder
Department of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 24 April 2015

ACKNOWLEDGEMENTS

I would first like to thank my research advisor Dr. Cressler. He has provided me with a multitude of research opportunities to investigate interesting topics and has been a source of support and encouragement in my work. I would also like to thank the members of my reading committee Dr. Papapolymerou and Dr. Yoder. They are both wonderful teachers in the classroom, and I appreciate the time they have taken to provide helpful feedback on my thesis work.

I also wish to thank all the current and past members of the SiGe Circuits and Devices team for creating a not only helpful but fun work environment over the years. I would like to offer particular thanks to Uppili and Partha for their advice and help in our shared reliability work.

I am very much grateful to Texas Instruments for the provision of hardware and software for furthering our work. Additionally, Keith Green, Hiroshi Yasuda, Jonggook Kim, and Philip Menz at TI have been invaluable for their advice and guidance in our monthly teleconferences.

Finally, I would like to thank my parents, Jane and Charles, for their support and love throughout the years.

TABLE OF CONTENTS

LIST OF FIGURES

SUMMARY

The objective of this work is to investigate and characterize different hot carrier degradation mechanisms in silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technologies.

In Chapter 1, the SiGe HBT is introduced and the need for predictive reliability modeling is motivated. The primary physical mechanisms for degradation in typical SiGe HBT operation are introduced and briefly discussed.

Chapter 2 presents an analysis of measured stress data and TCAD simulations for a first-generation SiGe HBT technology under high-current density operation. The damage behaviors seen are discussed within the context of hot carrier degradation and compared to mixed-mode degradation behaviors. The Auger recombination is pointed to as the hot carrier generation source, which is supported by the measured data and TCAD simulations. The analysis presented in Chaper 2 has been submitted to the IEEE Transactions on Electron Devices (TED) © 2015 [1].

Chapter 3 presents the beginning stages of a compact degradation model integrated with the Cadence Spectre circuit simulation environment. A physics based model has been formulated and calibrated using measured stress data and TCAD simulations. This reliability simulation capability will enable efficient prediction of end-of-life circuit performance, leading the way for reliability-aware circuit design.

In Chapter 4, a summary of the contributions presented in this thesis is given. In addition, future directions for comprehensive TCAD simulation of hot carrier stress effects and damage mitigation in circuit design through use of the compact degradation model is discussed.

CHAPTER 1

INTRODUCTION

In recent years, there has been incredible growth in the global telecommunications market, and at the core of that growth is the development of integrated circuit technologies that have enabled the production of high-performance systems for reasonable costs. Such growth is due to the constant scaling of core device performance metrics, and at the forefront of parameter scaling is the shrinking of both lateral and vertical device dimensions to achieve higher dynamic performance. A consequence of this continuous scaling, however, is the shrinking of the classical safe operating area (SOA) boundaries.

As circuit designers seek to maximize the circuit performance afforded by a given technology, device operating conditions are inevitably pushed to the edges of the DC-defined SOA boundaries. These SOA boundaries are conservatively defined by "soft" breakdown limits to ensure a circuit's reliable operation over its lifetime, meaning device operation can be pushed beyond these boundaries before the device undergoes catastrophic breakdown. With knowledge of the physics that drive device degradation outside the SOA, circuits can be designed to operate beyond classical SOA boundaries by limiting or mitigating the effects of individual device parameter shifts on overall circuit performance.

In order to understand how to design circuits that reliably operate outside the classical SOA, it is first necessary to thoroughly characterize and model the underlying processes involved in device degradation.

1.1 SiGe BiCMOS Technology

Modern silicon-germanium bipolar CMOS (SiGe BiCMOS) technology finds use

in a wide variety of analog/mixed-signal, RF, and high-speed digital circuits due to its high-frequency operation, low noise, high transconductance per unit area, and compatibility with normal CMOS fabrication techniques. A SiGe BiCMOS technology generally exists as a SiGe heterojunction bipolar transistor (HBT) available as an add-on to a digital CMOS technology. Integration of these two components allows for impressive integration on a single chip, with the SiGe HBT handling RF, microwave, and high-speed analog components and the Si CMOS handling memory and digital components. Recent SiGe BiCMOS platforms have demonstrated current-gain and power-gain cutoff frequencies (f_T and f_{max}) in excess of 300 GHz [2], and scaling trends support that THz SiGe HBTs with usable levels of breakdown should be possible [3]. This device performance level approaching that of III-V material technologies combined with the cost advantages of Si CMOS manufacturing make SiGe BiCMOS an ideal candidate for many growing applications.

1.1.1 The SiGe HBT

The modern SiGe HBT is fundamentally very similar to the standard Si bipolar junction transistor (BJT), but the HBT introduces a graded Ge profile in the base region. This Ge profile allows device designers to take advantage of bandgap-engineering in a silicon-based technology. The cross section of a representative first-generation silicon-germanium (SiGe) HBT is shown in Figure 1.1, and the corresponding doping profile for an *npn* device is shown in Figure 1.2. The energy-band diagram resulting from the introduction of the Ge profile (Figure 1.3) shows a graded offset that primarily occurs in the conduction band. The intrinsic band offset introduced by the Ge profile occurs in the valence band, but due to a p-type doped base layer, the energy offset between the Fermi level and the valence band is fixed. As the Fermi level must remain constant in equilibrium, the energy offset is instead shifted to the conduction-band edge.

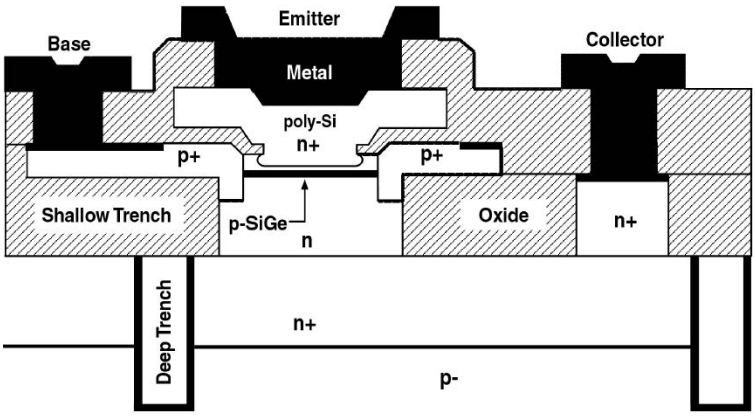


Figure 1.1: Cross-section of a representative first generation SiGe HBT (after [4]).

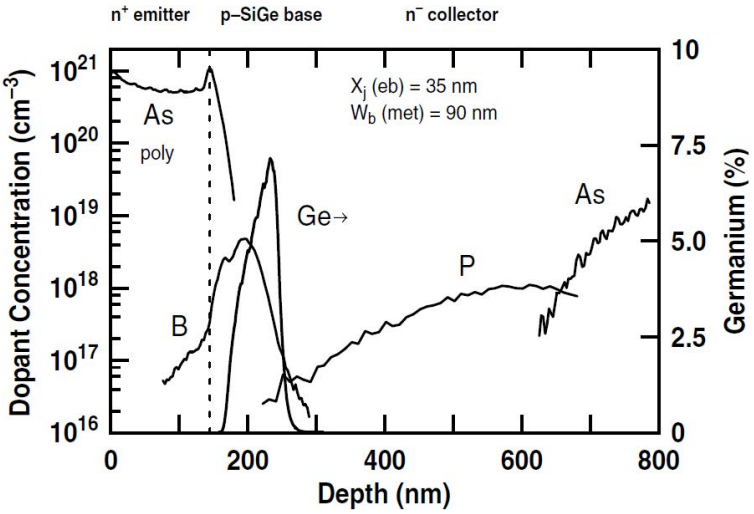


Figure 1.2: Measured SIMS profile of a representative first generation SiGe HBT (after [4]).

The introduction of the graded conduction band edge yields several improvements in DC operation of the SiGe HBT compared to the Si BJT. The Ge content at the emitter-base (EB) junction reduces the potential barrier for electron injection, which provides an exponential increase current conduction for the same bias which yields higher current gain. Additionally, output conductance is improved by a graded Ge profile. The graded bandgap within the base leads to a exponentially graded minority carrier profile, which for a bandgap minimum at the collector-base (CB) junction, weights the minority carrier profile such that backside depletion of the neutral base

is limited [4].

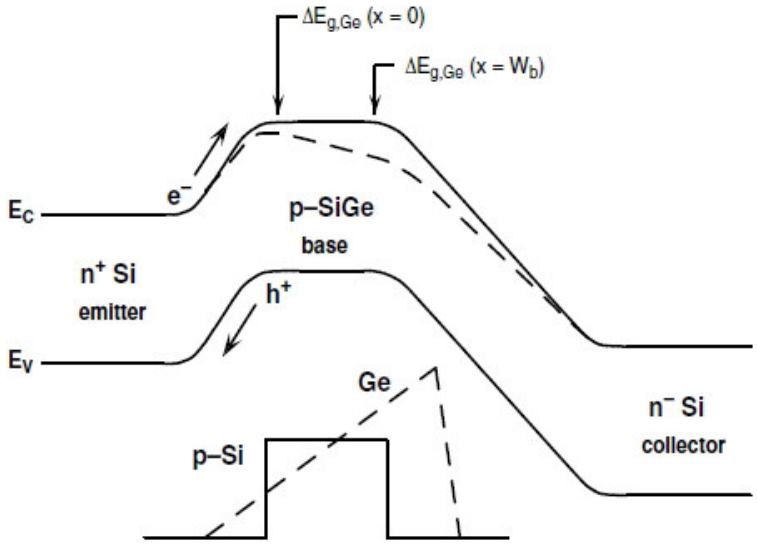


Figure 1.3: Energy-band diagram for a graded-base SiGe HBT (after [4]).

The graded Ge profile also leads to improvements in several AC performance metrics. The graded offset in the conduction band induces a drift field that boosts minority-electron transport across the base, reducing the base transit-time (τ_b), which is typically the limiting factor in determining unity gain frequency (f_T) and maximum oscillation frequency (f_{max}). Additionally, the enhancement of majority carrier mobility in the base layer due to the Ge content leads to a reduction in the base sheet-resistance (r_{bi}) [4].

1.1.2 Avalanche Multiplication

In order to take advantage of the potential for f_T afforded by the reductions in transit times by the Ge profile in a SiGe HBT, the collector current density (J_C) must be increased so that the charging times associated with the depletion and parasitic capacitances are minimized. At high J_C, however, the Kirk effect will cause the base region to "push-out" into the CB depletion region, effectively widening the base region and dramatically increasing τ_b. The Kirk effect begins when the charge density associated with current flow exceeds the charge density in the CB depletion region, so

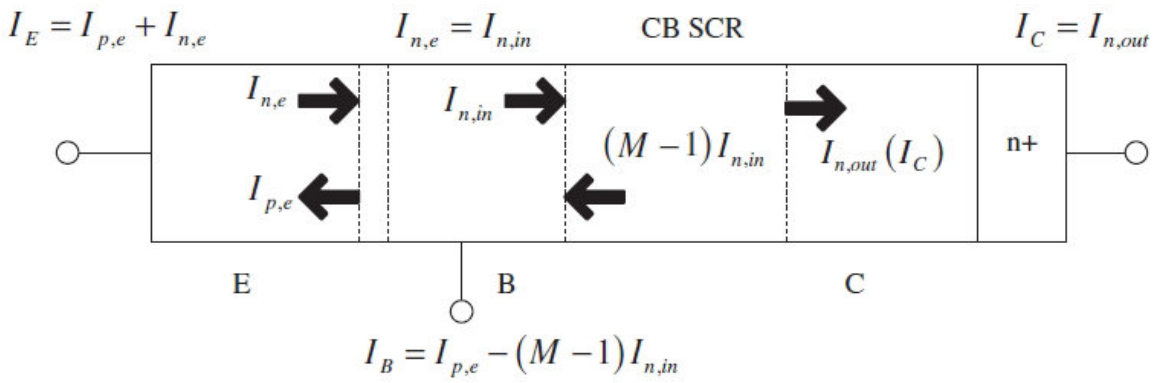


Figure 1.4: The avalanche multiplication process in a bipolar transistor under normal operation (after [4]).

to delay the onset of the Kirk effect, device designers will increase the collector doping. This increased doping in turn leads to an increase in the magnitude of the electric field in the CB junction. Under typical operation, the CB junction will be reverse-biased causing high impact-ionization rates. The resultant avalanche multiplication, which can be easily measured as the avalanche multiplication factor $(M-1)$, determines the breakdown voltage.

Avalanche multiplication in a bipolar device occurs by repeated impact ionization processes the CB depletion region. A basic diagram of the process is shown in Figure 1.4. Electrons injected from the base into the reverse-biased CB junction will be accelerated by the electric field and have a chance of undergoing impact ionization, where an energetic electron impacts the lattice with sufficient energy to generate an additional electron-hole (e-h) pair, and these secondary carriers can subsequently gain energy and undergo impact ionization. The result of this process is that the current leaving the CB junction is larger than the current entering the CB junction, and should the avalanching process be sufficiently strong, the excess current will cause the device to enter breakdown.

In this work $M-1$ is measured with a forced-I_E technique, where a current is forced in the emitter and the collector-base voltage (V_{CB}) is swept. We can determine the current entering the CB junction by using the fact that the I_B component due to

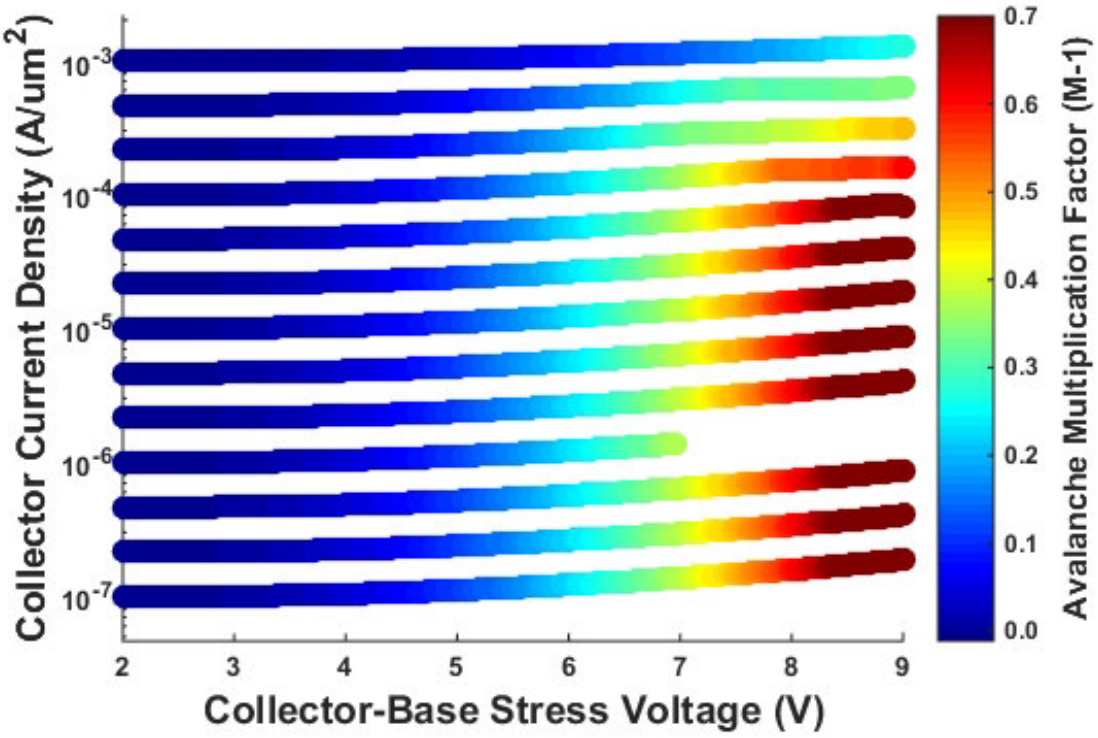


Figure 1.5: $M-1$ **data from a first-generation SiGe HBT measured using the force-**I_E **technique.**

hole injection is solely dependent on the base-emitter voltage (V_{BE}) and is equal to I_B for $V_{CB}=0$. With this consideration, $M-1$ can be expressed by [4]

$$M-1=\frac{I_{n,out}}{I_{n,in}}-1=\frac{I_C}{I_E-I_B(V_{BE})|_{V_{CB}=0}}-1. \tag{1.1}$$

As V_{CB} is increased, $M-1$ will naturally increase due to the increasing field in the CB junction. At high currents when the Kirk effect engages, the base pushout will lower the peak electric field in the junction, so $M-1$ will drop. Measured $M-1$ data for a wide range of bias conditions from a first generation SiGe HBT is shown in Figure 1.5.

1.2 Mixed-Mode Degradation

A common source of device degradation in both SiGe HBTs and Si CMOS technologies is trap creation at semiconductor/oxide interfaces by hot, or high-energy, charge carriers. In a SiGe HBT, this degradation will occur along the EB spacer oxide interface as well as the shallow-trench isolation (STI) oxide interface, which leads to an increase in the non-ideal base current due to increased trap-assisted Shockley-Read-Hall (SRH) recombination. In a typical mixed-signal circuit, a SiGe HBT is particularly vulnerable to the mixed-mode damage mechanism, which results from simultaneous application of high J_C and high V_{CB} [5]. The mixed-mode damage mechanism has a complex response to circuit operating conditions with distinct damage and annealing regions determined by the time-dependent electric field, lattice temperature, and current densities within the device [6].

In order to predict the device degradation over time, an understanding of hot carrier driven trap creation is necessary. Hot carrier degradation relies on two major processes: 1) the generation of hot carriers and their transport to an oxide interface, and 2) the formation and annealing of traps at that interface [7]. These processes, shown schematically in Figure 1.6, occur under traditional mixed-mode stress conditions when minority carriers from the base enter the CB depletion region from the base and are accelerated by the high electric field. These carriers can gain sufficient energy to undergo impact ionization, creating additional energetic pairs. These newly generated hot carriers can then proceed to participate in additional impact-ionization events, creating an avalanche effect. Throughout this process, energetic carriers can be redirected towards an oxide interface, and if these carriers reach the oxide with sufficient energy, they can de-passivate dangling bonds at the interface and create trap states [7]. Traps will generally be created at the EB spacer oxide and STI oxide interfaces, increasing the non-ideal base current in forward-mode and inverse-mode

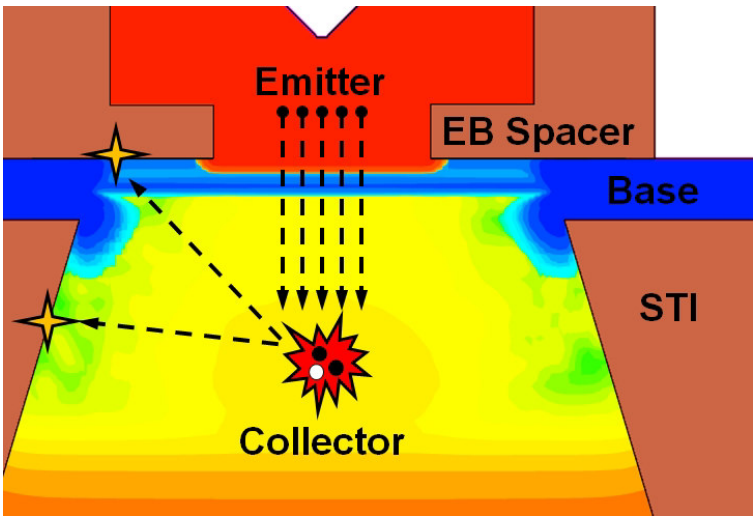


Figure 1.6: 2-D cross-section of a SiGe HBT model depicting the basic process of the mixed-mode degradation mechanism (after [8]).

(electrical emitter and collector swapped), respectively, due to increased SRH recombination. As the effects on the forward-mode operation are more relevant to typical circuit operation, the traps generated at the EB spacer oxide are of greater concern.

The generation and transport of hot carriers has commonly been modeled using the lucky-electron model (LEM), which applies individual probabilities to each step in that process [9,10]. The LEM determines the rate at which hot carriers impinge on the oxide interface as the product of: 1) the local carrier density; 2) the probability that a carrier gains sufficient energy to generate a trap state; 3) the probability that a hot carrier will be redirected toward the oxide interface with sufficient momentum; and 4) the probability that a hot carrier will reach the oxide interface without undergoing an energy-robbing collision. The hot carrier probability P_{hot} derived from mixed-mode stress conditions is driven by the effective electric field F_{eff}, and is defined as

$$P_{hot}(\epsilon, x, y) = \int_{\phi_{hot}}^{\infty} \frac{1}{\lambda F_{eff}(x,y)} e^{-\epsilon/\lambda F_{eff}(x,y)} d\epsilon \tag{1.2}$$

where λ is the carrier mean-free-path length, and ϕ_{hot} is the threshold energy required to de-passivate a dangling bond [8]. Here $F_{eff}(x, y)$ is computed based on a

conversion from the local carrier temperatures in the hydrodynamic transport model [11].

Once at an oxide interface, trap formation by hot carriers is caused by de-passivation of silicon dangling bonds along the interface. The reaction-diffusion (R-D) model has typically been used to explain the hydrogen-diffusion-controlled surface state creation mechanism of bias temperature instability [12], but the same model can be successfully applied here [8]. The evolution of the interface trap density N_{it} can be computed from the R-D formalism

$$\frac{\partial N_{it}}{\partial t} = K_F(N_0 - N_{it}) - K_R N_{it} H_2 \tag{1.3}$$

where K_F is the forward reaction rate determined by the hot carrier probabilities, K_R is the reverse reaction rate, N_0 is the total dangling bond density at the interface, and H_2 is the hydrogen density at the interface [12]. In a forward-reaction-dominated process far from saturation, such as a mixed-mode stress condition, an approximate solution to (1.3) gives [8, 12]

$$N_{it}(t) \approx 1.16\sqrt{\frac{K_F N_0}{K_R}}(Dt)^{\alpha} \tag{1.4}$$

where D is the diffusion coefficent of hydrogen in the oxide and α sets the power-law time dependence of trap formation. A $t^{0.25}$ time dependence where $\alpha = 0.25$ matches the degradation trend seen in [12].

CHAPTER 2

HOT CARRIER RELIABILITY AT HIGH-CURRENT DENSITY OPERATION

2.1 Introduction

As SiGe BiCMOS technologies continue to find use in high-speed analog/mixed-signal and RF applications, combined optimization of the lateral and vertical scaling of SiGe HBTs is needed to obtain improved dynamic performance. A consequence of this continuous scaling driven by the desire for greater performance is the shrinking of classical SOA boundaries. In order to achieve higher peak f_T, an increase of the collector doping is needed to suppress the Kirk and heterojunction barrier effects. This increase in doping, however, leads to a strong increase in the CB junction field and to an increase in the J_C needed to reach peak f_T. As circuit designers seek to maximize the circuit performance afforded by a given SiGe technology platform, operating conditions are inevitably pushed nearer and nearer to the DC-defined SOA boundaries. Because of this, an understanding of the physics that determine the time-to-failure (TTF) for a circuit is necessary.

The main concern with end-of-life performance of a circuit is how circuit parameters shift due to transistor degradation over time. A common degradation mechanism is the generation of interface traps at the EB spacer oxide and the STI oxide by hot, or high-energy, charge carriers, which causes the base current to increase over time (i.e., degrade). Hot carrier degradation is generally caused by the mixed-mode degradation mechanism [5, 13], which can be traced to the generation of hot carriers by large electric fields in the CB junction under simultaneous high V_{CB} and moderate

J_C biasing conditions. Interestingly, similar hot carrier driven interface trap generation has also been seen under simultaneous low-voltage and high-current stress conditions, where electric fields are not large enough to produce hot carriers. Some studies have suggested Auger generation as a candidate mechanism for hot carrier generation under such stress conditions [14–17], and in [18], we provided evidence to support Auger generation as the driving mechanism. This work expands upon that previous study through explanation of the role Auger recombination plays in hot carrier degradation, comparison of the effects of mixed-mode stress and high-current stress, and explanation for the different behaviors attributed to Auger recombination seen in high-current stress using stress measurement data and calibrated technology computer aided design (TCAD) simulations.

2.2 Hot Carrier Physics

In order to understand the differences between mixed-mode and high-current stress degradation, we first look to the previously established hot carrier framework of the lucky-electron model (LEM) and the reaction-diffusion (R-D) model and examine the driving procesess:

1. The generation of hot carriers and their transport to an oxide interface.

2. The formation and annealing of traps at that interface.

When examining degradation under high-current stress, we see an increase in the non-ideal base current and time dependence similar to those of mixed-mode degradation. This similarity suggests that assuming the same framework for high-current degradation physics is reasonable. Under low-voltage, high-current stress, the large electric field needed to produce hot carriers is missing, but if another mechanism is capable of producing hot carriers, then it is reasonable to assume that the proceeding processes of re-direction, travel to an oxide interface, and de-passivation of a dangling bond are

the same. A prevalent process and likely source of hot carriers under high-current operation is Auger recombination, wherein an electron-hole pair recombines and a third free carrier is subsequently accelerated to higher energy. In a SiGe HBT, Auger generation should not be able to provide the energy required to de-passivate a silicon dangling bond at the oxide interface (2.3 eV [7]), but with a sufficient carrier density, repeated recombination processes involving the same carrier should be able to provide a sufficiently large thermal tail to the carrier energy distribution function (EDF), which shows a Maxwellian shape [19].

Similar to the avalanching impact-ionization process that plays a large role in mixed-mode degradation, a possible avalanching of the Auger process, which is essentially the inverse process to impact ionization, would provide sufficient energy for hot carrier degradation. Studies of hot carrier injection in MOSFETs have shown that Auger recombination and the similar electron-electron scattering process can contribute to hot carrier degradation under certain conditions [17,20]. Though it has reduced probability of creating hot carriers with sufficient energy, the Auger generation degradation process is enhanced relative to mixed-mode degradation due to the physical location where these processes occur within the device. The highest rates of Auger generation occur in the EB depletion region or within the neutral base, as opposed to the CB depletion region for high fields in mixed-mode stress. Given the increased proximity to the EB spacer oxide of Auger generated hot carriers, the probability of energy-robbing collisions is reduced exponentially because hot carriers have to travel a shorter distance [8].

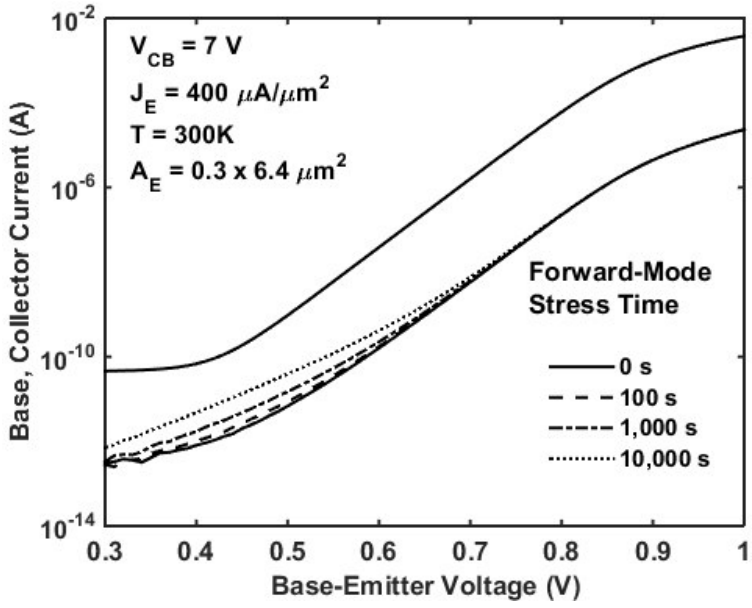
2.3 Device Stress Measurements

The devices used in this investigation were first-generation SiGe HBTs from a 0.3 μm commercial complementary SiGe HBT technology with a 50 GHz peak f_T

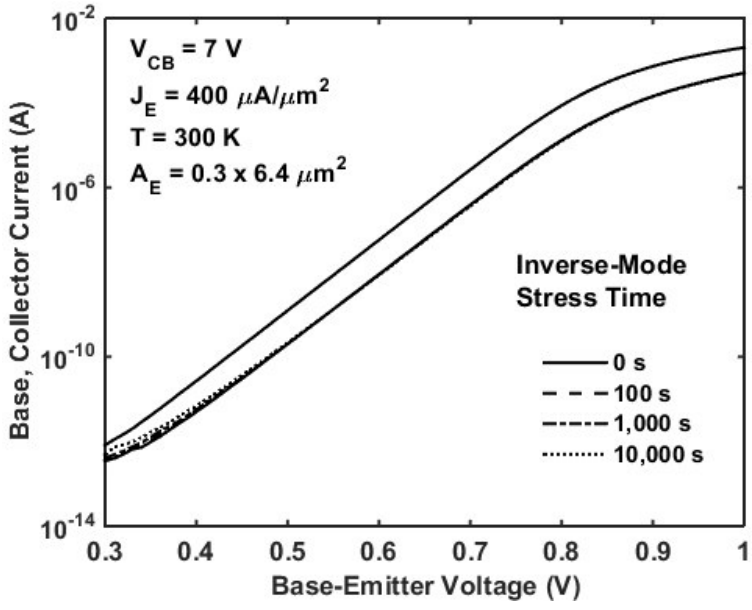
at J_C of about $1 - 2\ mA/\mu\text{m}^2$, and a minimum open-base collector-emitter breakdown voltage (BV_{CEO}) of 3.3 V. Measurements were performed on-wafer using an automated DC probing system equipped with a hot-chuck for over temperature measurements. Transistors were stressed using an Agilent 4155C Semiconductor Parameter Analyzer by pulling a set current density through the emitter and applying a set reverse-bias voltage across the CB junction with the base grounded for a predetermined time interval. Device degradation was monitored by periodically interrupting the stress and measuring forward-mode and inverse-mode Gummel characteristics. Each stress condition was measured on a fresh unstressed device.

2.3.1 Mixed-Mode Stress

We briefly examine mixed-mode stress data to set a baseline for comparison with the high-current stress results. A stress condition representative of peak avalanche generation in mixed-mode stress is shown in Figure 2.1, which shows the time evolution of a device's forward and inverse Gummel characteristics, over $10,000$ s, for a stress bias of $J_E = 400\ \mu A/\mu m^2$ and $V_{CB} = 7\ V$. As expected for a high-voltage stress condition, the non-ideal base current in both the forward-mode and inverse-mode Gummel characteristics increases, which indicates the formation of interface traps at the EB spacer oxide and at the STI edge. We measured the degradation of these devices across a large set of bias points in the mixed-mode stress region, and as seen on the stress map shown in Figure 2.2, mixed-mode stress follows the same bias dependency as avalanche generation. That is, base current degradation increases with voltage due to increased impact ionization rates and hot carrier probability, and the degradation increases with current due to the increase in available carriers to participate in damage physics, but then decreases rapidly at high currents due to the Kirk effect, which lowers the maximum electric field and pushes the hot carrier generation location away from the EB spacer oxide. Trap creation along the STI



(a)



(b)

Figure 2.1: Mixed-mode stress evolution over $10,000$ s for the stress condition $J_E = 400\ \mu A/\mu m^2$ and $V_{CB} = 7\ V$. The (a) forward-mode and (b) inverse-mode Gummel characteristics show the effects of interface traps at the EB spacer oxide and STI oxide, respectively.

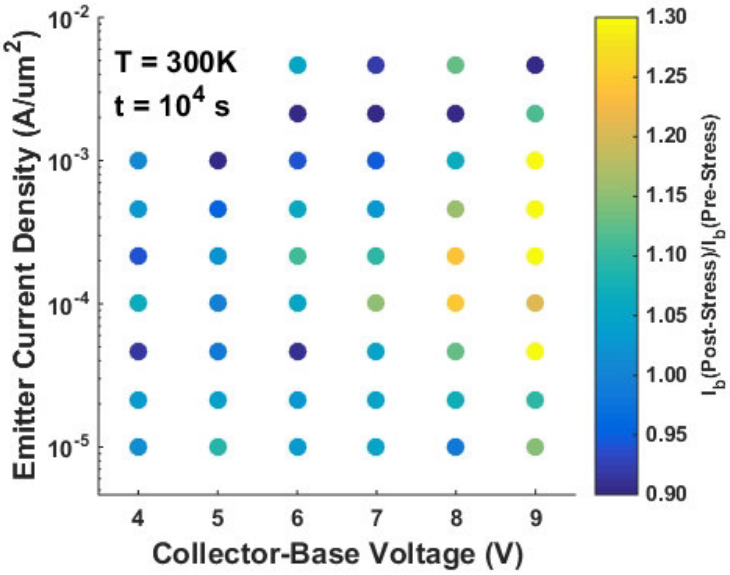
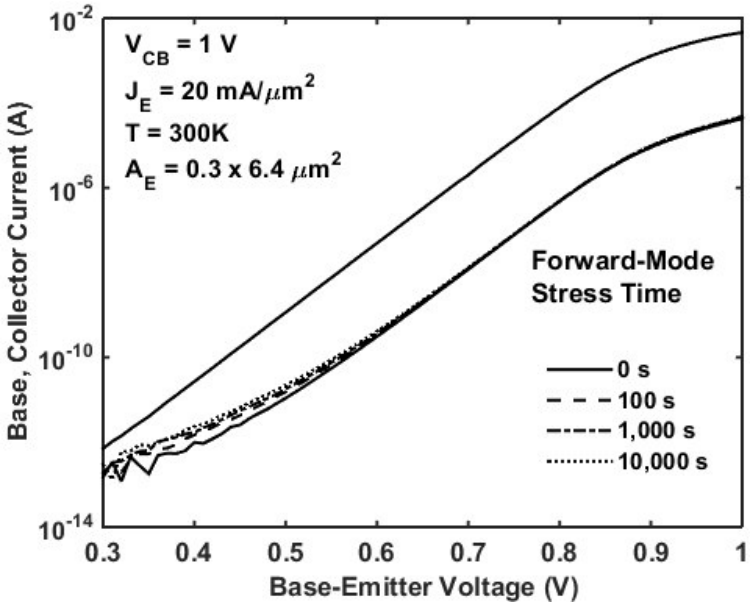


Figure 2.2: Mixed-mode stress map showing the ratio of post-stress and pre-stress base current after $10,000$ s for a wide range of stress conditions taken from forward-mode Gummel characteristics at $V_{BE} = 0.5\ V$.

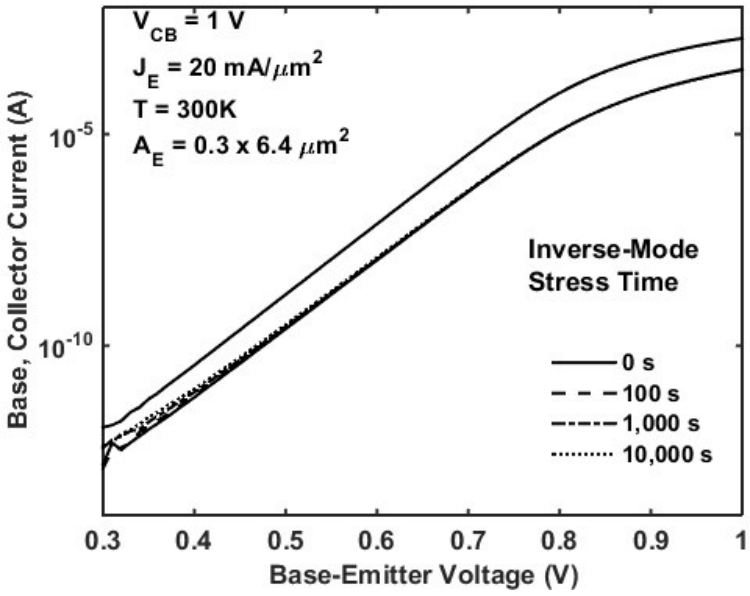
oxide, however, will continue to increase with current density despite the Kirk effect because the hot carrier generation location moves along, not away from, the interface. A more detailed explanation on the bias dependencies of mixed-mode stress in the framework of the LEM is shown in [8].

2.3.2 High-Current Stress

Using the same setup utilized during mixed-mode stress, we biased devices at current densities larger than J_C at peak f_T, and to isolate the effects of high-current damage, stress voltages were kept small to minimize the contribution of field-generated hot carriers to trap generation. The evolution of the Gummel characteristics over $10,000$ s, for a representative high-current stress bias of $J_E = 20\ mA/\mu m^2$ and $V_{CB} = 1\ V$, is shown in Figure 2.3, where an increase in the non-ideal base current is apparent, and which is indicative of interface trap creation at the EB spacer and STI oxides.



(a)



(b)

Figure 2.3: High-current stress evolution over $10,000$ **s for the stress condition** $J_E = 20\ mA/\mu m^2$ **and** $V_{CB} = 1\ V$**. The (a) forward-mode and (b) inverse-mode Gummel characteristics show the effects of interface traps at the EB spacer oxide and STI oxide, respectively.**

Upon closer inspection of the Gummel characteristics, additional current shifts are visible. As shown in Figure 2.4, there is a small initial decrease in the ideal base current as well as an eventual increase in both the collector and base current

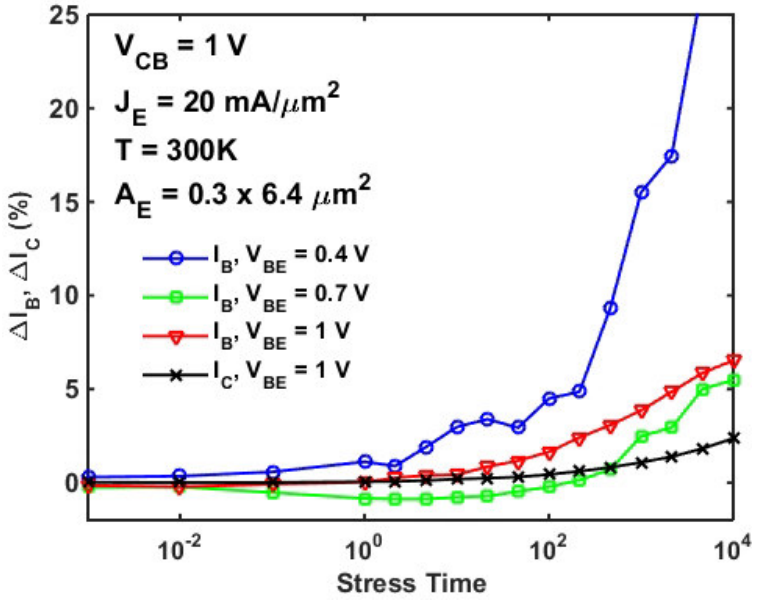


Figure 2.4: Time evolution of base and collector current for the stress condition $J_E = 20\ mA/\mu m^2$ and $V_{CB} = 1\ V$. Non-ideal base current shifts are evident at low V_{BE} and shifts in the ideal base current and R_E are evident for high V_{BE}.

for high values of V_{BE}. This has previously been attributed to an annealing process of interface traps at the poly-silicon/crystalline-silicon emitter interface that reduces recombination at the interface and leads to a decrease in the emitter resistance (R_E) [15,16]. The previous studies have reported current shifts as high as 30% in a Silicon BiCMOS platform [15] and $15-20\%$ in a higher performance SiGe HBT platform [16]. As explained in [15], the degradation and annealing processes are primarily dependent on the quality of the interface and the availability of atomic Hydrogen, and as such, we can infer that the difference in these changes can be attributed to a difference in interface quality across different technologies. Additionally, an effect involving the Germanium profile that leads to increased damage, explained in the next section, also contributes to the difference compared to the Silicon BiCMOS platform presented in [15]. As these devices show minimal annealing behavior, the changes in the non-ideal base current due to trap creation will overtake the effects of the annealing over time.

As we look at the effects of high-current stress over a wider range of stress conditions, a few different behaviors become apparent. When examining the degradation

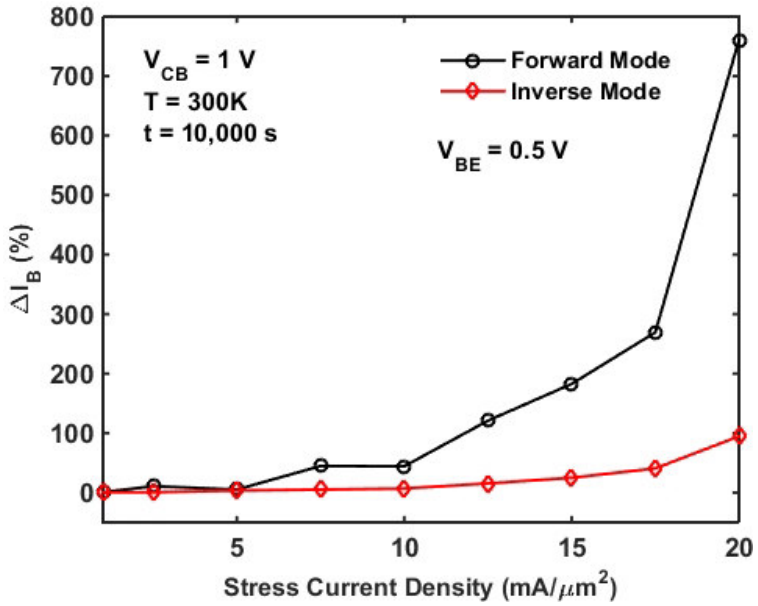


Figure 2.5: Base current degradation at $V_{BE} = 0.5\ V$ on forward Gummel characteristic after $10,000$ s for $V_{CB} = 1\ V$ and a range of stress current densities.

over a range of current densities, an interesting threshold appears around a stress current density of 10 $mA/\mu m^2$, as shown in Figure 2.5. For a stress below 10 $mA/\mu m^2$, the base current indicates both damage and annealing behaviors over time. Referring to the R-D formalism, we can infer that there is a range of current values where the forward and reverse reaction rates, K_F and K_R, are balanced. The reverse reaction process is driven by the availability of hydrogen species in proximity of the oxide interface and is greatly affected by temperature [12]. At high current densities, self-heating within the device can become significant, leading to an increased reverse reaction; however, it is clear that above a certain current density, the forward reaction process begins to dominate. The cause of this behavior is discussed in the next section. Figure 2.5 also shows that degradation of the inverse mode is significantly less than forward mode degradation, which is due to the STI oxide interface being located farther away from the region of peak Auger regeneration in the EB depletion region and the neutral base.

As the stress voltage is increased while maintaining a very high current density,

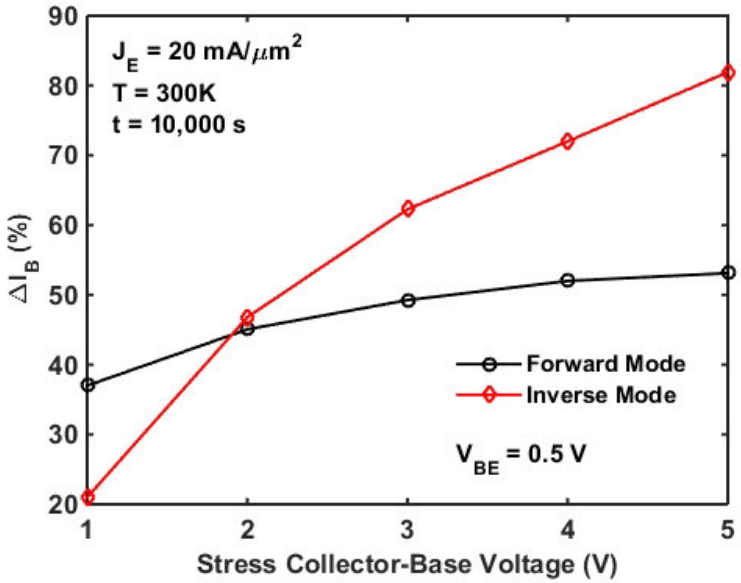


Figure 2.6: Base current degradation at $V_{BE} = 0.5\ V$ on inverse Gummel characteristic after $10,000$ s for $J_E = 20\ mA/\mu m^2$ and a range of stress voltages.

an expectation that the forward mode damage should increase as the mixed-mode mechanism begins to contribute would be reasonable; however, minimal change in the damage at the EB oxide occurs, as seen in the forward mode data in Figure 2.6. Considering the Kirk effect is strongly engaged, causing the maximum electric field to decrease and push deep into the device away from the EB oxide interface, the observed negligible damage increase is reasonable. Additionally, Auger recombination is largely dependent on the carrier densities and independent of the electric field. If we instead focus on the inverse-mode operation, damage does in fact increase consistently with voltage, as shown in Figure 2.6. As the increased damage occurs for stress voltages as low as $4\ V$, for which typical mixed-mode damage at the EB oxide is small in this technology, evident in Figure 2.2, this behavior requires further investigation through the use of TCAD for explanation.

With an increase in operating temperature, the effects of mixed-mode degradation will decrease due to decreased avalanche generation and an increased probability of

scattering due to a shortened mean-free-path length. Because the scattering and redirection probabilities for Auger hot carriers are similar to those for mixed-mode hot carriers, a similar temperature dependence would be expected. However, an increase in Auger hot carrier degradation is observed with increasing temperature. This can be seen in Figure 2.7, where the degradation for a single stress condition of $V_{CB} = 2\ V$ and $J_E = 20\ mA/\mu m^2$, measured at both $25°C$ and $100°C$, is shown. The higher temperature stress condition clearly develops damage at a faster rate. The comparison is made here by looking at the relative change in the Gummel characteristics from each temperature sampled at an initial base current of $I_B = 1\ pA$, depicted in the inset of Figure 2.7, which allows for isolating the degradation from the effects of the difference in temperatures. This current value was chosen to sample an operating point at which interface traps contribute significantly to the total base current. There are two factors that account for this temperature dependence with Auger hot carriers: the Auger recombination rate, and the hot carrier EDF. Previous studies show that Auger recombination rates will increase by about $20 - 50\%$ depending on the carrier density over this temperature range [21, 22]. An increase in recombination rates means an increase in the number of hot carriers generated. Additionally, due to the thermalized energy tail of the Auger recombination EDF, increased temperatures will increase the probability that charge carriers excited by the Auger process have sufficient energy to create trap states.

2.4 High Current Simulations

We have simulated high-current device operation using a well-calibrated 2-D device profile in the Synopsys Sentaurus TCAD suite in order to further investigate two interesting behaviors seen in high-current stressing: 1) the threshold behavior seen around 10 $mA/\mu m^2$, and 2) the effect of stress voltage during high-current operation on inverse-mode degradation.

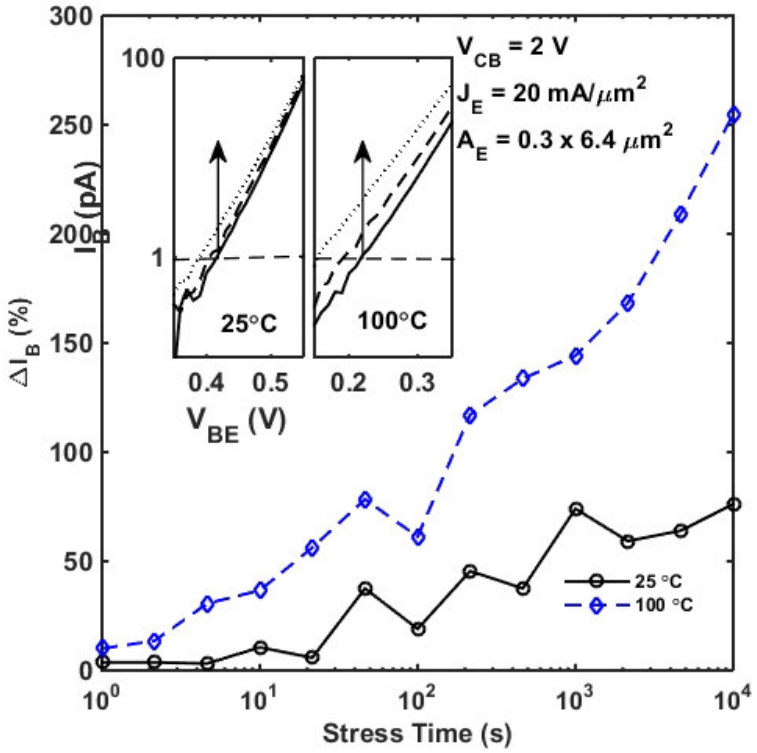


Figure 2.7: Base current degradation extracted from forward-mode Gummel characteristics at $I_B = 1\ pA$ for the stress condition $V_{CB} = 2\ V$ and $J_E = 20\ mA/\mu m^2$ at both $25°C$ and $100°C$.

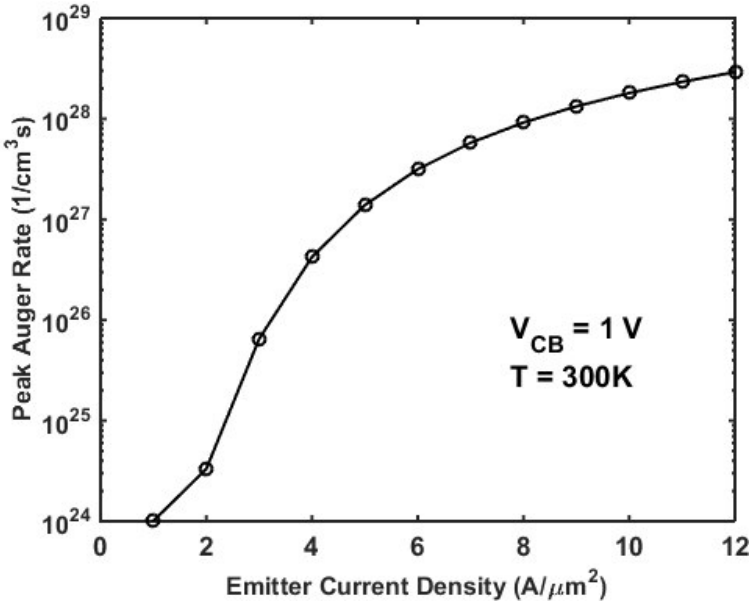


Figure 2.8: TCAD simulated peak Auger recombination rate within the neutral base region.

By comparing Auger recombination rates within the device across current density, the underlying reason for the threshold behavior becomes evident. From $1 - 10\ mA/\mu m^2$, Auger recombination within the neutral base increases several orders of magnitude, and with hot carriers being created closer to the EB spacer oxide, the trap formation rate will increase. Shown in Figure 2.8, the peak Auger recombination rate within the neutral base increases sharply until $J_E = 6\ mA/\mu m^2$. The cause of this increase is the exposure of the triangular Germanium profile utilized in the base at the onset of the Kirk effect, which creates a potential well in the neutral base region, as shown in Figure 2.9.

To investigate the trap formation at the STI oxide interface, which appears as damage in the inverse-mode Gummel characteristics, we must observe what happens to the electric field within the device as the current is increased. Figure 2.10 shows the electric field within the collector for increasing current densities. Strong Kirk

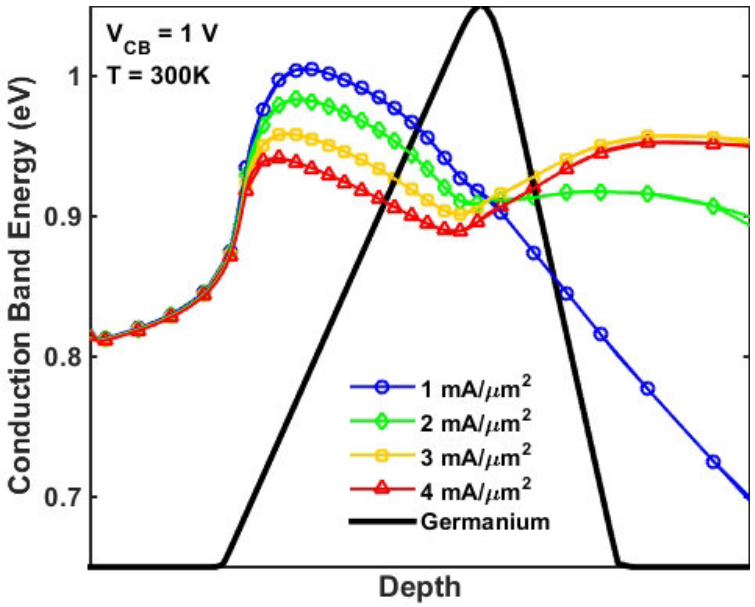


Figure 2.9: TCAD simulated conduction band energy in neutral base region for a range of current densities with the Germanium profile shape overlaid.

effect is evident, as expected, and the electric field is pushed deeper into the collector region. At sufficiently high current density, the field will be pushed all the way to

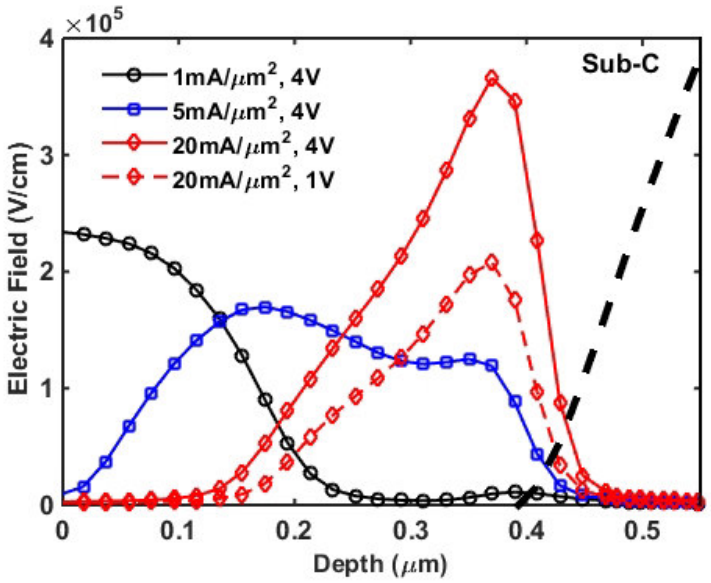


Figure 2.10: TCAD simulated electric field in the collector region for $V_{CB} = 4\ V$ for a range of emitter current densities demonstrating compression of the electric field at the subcollector under heavy Kirk effect. Additionally, the field at $J_E = 20\ mA/\mu m^2$ and $V_{CB} = 1\ V$ is shown for comparison. The location of the subcollector is shown by the heavy dashed line.

the sub-collector region. Once the field is pushed to the sub-collector, it will begin to compress and the applied V_{CB} potential drop will occur over a narrow region, leading to enhanced hot carrier generation and impact ionization, consistent with our data. The enhanced hot carrier generation is evident in the inverse mode data in Figure 2.5, which shows a sharper increase in inverse-mode damage beyond 10 $mA/\mu m^2$.

2.5 Summary

We have investigated high-current electrical stress degradation in SiGe HBTs, and compared the process to traditional mixed-mode stress degradation. We have concluded that the non-ideal base current formation seen under high-current stress is also due to trap formation at the EB spacer oxide and STI oxide interfaces by hot carriers. We have provided evidence that the Auger recombination process is the source of hot carriers under high-current conditions, and explained how it couples with the hot carrier and trap formation physics. Measurements over a range of stress

conditions have revealed a number of differences on bias dependency between high-current stress and mixed-mode stress. High-current stress damage increases with current density and exhibits a threshold behavior attributed to the formation of a potential well in the neutral base during base pushout, which leads to a sharp increase in Auger recombination within the neutral base. Trap formation at the STI oxide interface was also observed to have a stronger than expected voltage dependence as a result of a compression of the electric field at the collector/sub-collector interface under Kirk effect. Additionally, Auger hot carrier degradation displays a positive temperature dependence, unlike mixed-mode stress, due to the nature of the Auger recombination mechanism.

CHAPTER 3

COMPACT MODELING OF MIXED-MODE DEGRADATION

3.1 Introduction

How to accurately and efficiently predict end-of-life circuit performance remains an open question in the world of semiconductor modeling, and the ability to quickly look at the end-of-life response for a circuit remains as a sort of "holy grail" for circuit designers. The underlying problem though is highly sophisticated, and while circuit designers treat the transistor as a perfectly modeled black box, it is not that simple. Device reliability and aging is a complex response to the dynamic operating conditions of a device over its lifetime. A multitude of efforts have been made to capture the aging behavior of specific degradation mechanisms, such as bias temperature instability (BTI) [12] and hot carrier injection (HCI) [9, 10] in MOS devices as well as mixed-mode degradation in bipolar devices [8, 23], using TCAD solutions that can calculate the electric field and carrier densities of a device under dynamic operating conditions. This is truly the only way to make predictions that account for all the relevant physics, but accurate reliability simulation for a device can take a long period of time, making TCAD simulation of a full circuit prohibitively long for use by circuit designers. Long term reliability prediction for a bipolar device is particularly difficult due to the number of competing degradation mechanisms as the device operating point swings through several different damage regions. Figure 3.1 shows a representative dynamic load-line for a device in a cascode power amplifier passing through multiple degradation regions.

The most practical step towards achieving fast circuit reliability in a simulation

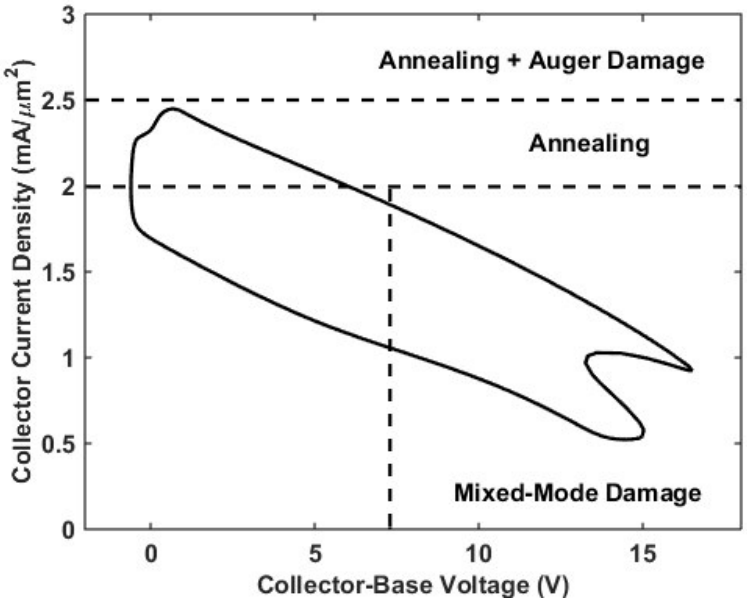


Figure 3.1: TCAD simulated dynamic loadline for the upper device in a SiGe HBT cascode amplifier. Approximate demarcations of different damage regions show the variety of stress conditions this device will go through during its operation (after [24]).

environment is the development of a stress damage wrap-around for a device compact model. While it will fail to capture the full physics of the stress environment such as in TCAD, the stress damage model should be physics based and can be informed by calibrated TCAD stress simulations. Similar approaches have been made in the past with some success, such as for hot carrier breakdown of CMOS devices [25, 26], but most models fail to present the full picture for circuit aging, either through the use of simple physical models or incomplete representation of aging effects in the device [27, 28]. This work represents the first steps in the development of a physics based damage model as a wrapper for SiGe HBT compact models that will cover the major components of hot carrier degradation. Here we use the framework of the coupled lucky-electron model (LEM) and reaction-diffusion (R-D) model to formulate analytic degradation equations for mixed-mode stress and incorporate them into the Cadence Spectre circuit simulator.

3.2 Model Formulation

The primary result of mixed-mode degradation in a SiGe HBT is an increase in the non-ideal base current due to an increase in interface traps at the EB spacer oxide and the STI oxide. The processes behind this degradation have successfully been simulated in a TCAD environment using a modified version of the LEM [8, 23]. The LEM shows that the degradation rate is dependent on the rate at which hot carriers impinge on the relevant oxide interfaces. Using a combination of measured and simulated stress data, the individual probabilities that determine the hot carrier rates can be converted to simpler forms based on the device operating point. The first probability to consider is the probability that a charge carrier will become hot [9]

$$P_{hot} = \int_{\phi_{hot}}^{\infty} \frac{1}{\lambda E} e^{-\frac{\epsilon}{\lambda E}} d\epsilon = e^{-\frac{\phi_{hot}}{\lambda E}} \tag{3.1}$$

where λ is the carrier mean-free-path length, E is the electric field, and ϕ_{hot} is minimum energy required to break a dangling bond at the oxide/semiconductor interface. By inspection, (3.1) has the same form as the probability for impact-ionization to occur, which leads to the conclusion that the two probabilities are proportional. This information then allows us to use the avalanche generated current I_{avl} as a measure for the total number of hot carriers generated

$$HC = \frac{1}{q} I_{avl} \cdot e^{-\frac{\phi_{hot} - \phi_{II}}{\lambda E_{max}}} \tag{3.2}$$

where q is the electron charge, ϕ_{II} is the threshold energy for impact ionization, E_{max} is the peak electric field in the junction. Modern bipolar compact models such as HICUM and MEXTRAM accurately model avalanche current in the device, so I_{avl} can be extracted directly from the model. By approximating the CB junction as a one-sided $p^+ - n$ junction, we can make an approximation on the peak electric field

E_{max} to simplify (3.2) and condense it to an external bias dependent form

$$HC = \frac{1}{q} I_{avl} \cdot e^{-b\sqrt{\frac{1+I_E/I_1}{V_{bi}+V_{CB}}}} \tag{3.3}$$

where b and I_1 become model fitting parameters for the model and V_{bi} is the built-in voltage of the CB junction. The I_E dependence is included as an approximation for the current at the BC junction and is used to model the lowering of the peak electric field at high current densities when the Kirk effect engages.

The remaining probabilities for the LEM are the probability that a hot carrier is redirected toward an oxide interface and the probability that a carrier reaches the oxide interface without undergoing an energy-robbing collision. In an *npn* device, hot holes are naturally directed toward the EB spacer from the CB depletion region, and measurements done to determine the redirection probability have found that the fraction of electrons redirected toward the EB spacer can be simplified to a small constant [29]. Under these assumptions, the total redirection probability can be taken as a constant. The collision probability is given by $e^{-d/\lambda}$ [10], where λ is the mean-free-path length and d is the distance the hot carrier must travel. If we take d to be the distance from peak electric field to the EB spacer, the collision probability will remain constant at low current densities. Taking the shift in the peak location to be linear with current density [30], the collision probability becomes

$$P_{coll} \propto e^{-\frac{I_E}{I_0}} \tag{3.4}$$

where I_0 is an additional model fitting parameter. Combining (3.3) and (3.4), the total hot carrier impingement rate at the EB spacer becomes

$$HC_{EB} = A_0 \frac{1}{q} I_{avl} \cdot e^{-b\sqrt{\frac{1+I_E/I_1}{V_{bi}+V_{CB}}}} e^{-\frac{I_E}{I_0}} \tag{3.5}$$

where A_0 is a model fitting parameter.

With an accurate approximation for the hot carrier rate, taking that to be the forward reaction rate in the R-D model yields a solution for the time evolution of the interface traps as in (1.4). As the SRH recombination current is directly proportional to the interface trap density, an equation for the degradation of the non-ideal base current in the device is directly obtainable as

$$\Delta I_{SRH} = I_{SRH,0} \cdot A_0 \sqrt{I_{avl} \cdot e^{-b\sqrt{\frac{1+I_E/I_1}{V_{bi}+V_{CB}}}} e^{-\frac{I_E}{I_0}} \cdot t^n} \tag{3.6}$$

where $I_{SRH,0}$ is the original SRH recombination current.

Using measured and TCAD simulated stress data, this model has been fit to a 2^{nd}-generation SiGe HBT technology. A comparison of hot carrier rates obtained from TCAD simulations and the proposed model for a wide range of stress bias conditions is shown in Figure 3.2. Good fit is seen between the model and TCAD up to current densities above J_C at peak f_T ($1\ mA/\mu m^2$). In comparison to measured data, excellent fit is also seen. Figure 3.3 shows great fit of the time dependence of the model up to $10,000$ s, and Figure 3.4 shows good fit for a range of bias conditions.

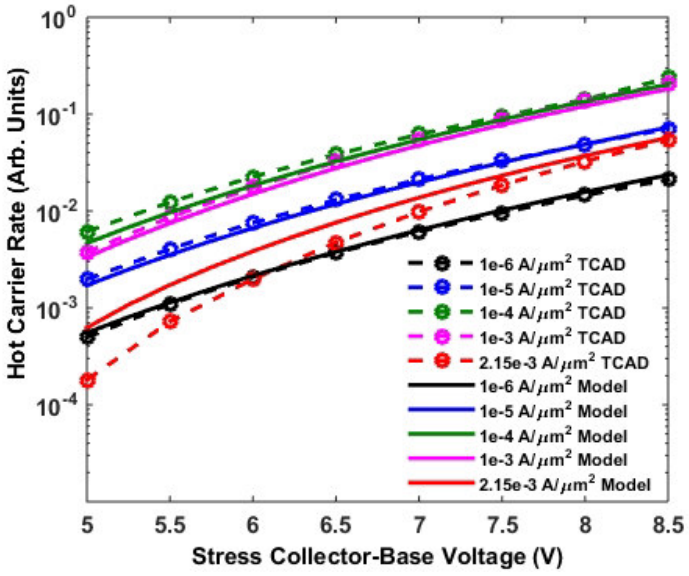


Figure 3.2: Stress model and TCAD calculated hot carrier rates for a wide range of stress bias conditions.

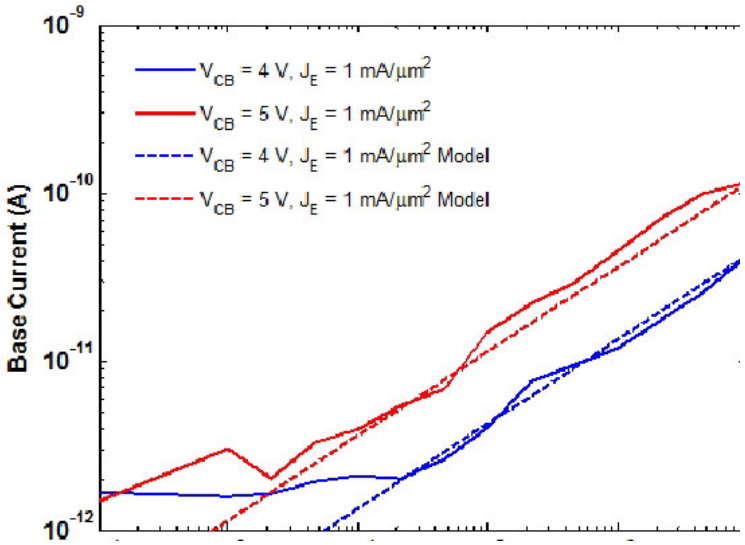


Figure 3.3: Comparison of stress model to measured data for the stress conditions $V_{CB} = 4\ V$ and $V_{CB} = 5\ V$ with $J_E = 1\ mA/\mu m^2$ measured up to $10,000$ s.

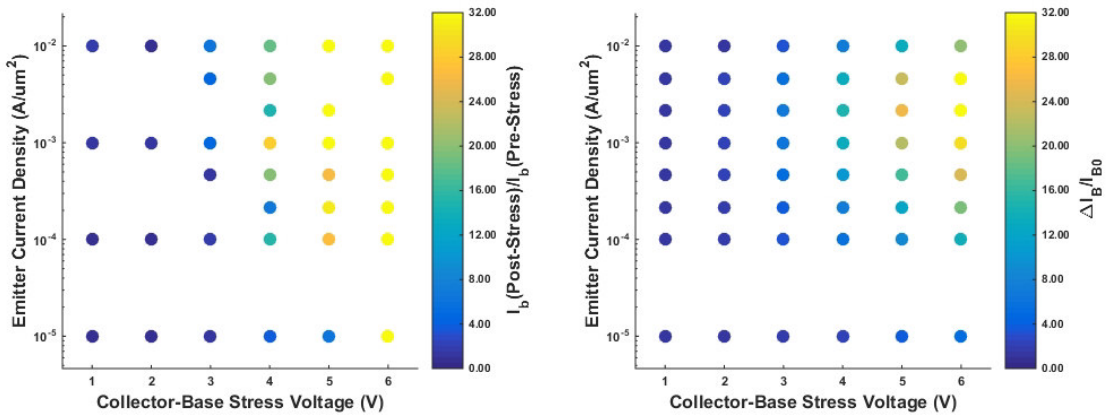


Figure 3.4: Stress maps for $10,000$ s mixed-mode stress in a second-generation SiGe HBT measured at $V_{BE} = 0.5\ V$ in the forward-mode Gummel characteristic for (a) measured data and (b) model data.

3.3 Simulation Framework

The degradation has been implemented in the Cadence Spectre circuit simulation environment via the Unified Reliability Interface (URI) framework [31]. The Spectre URI allows externally defined reliability models to be implemented as wrappers around the the simulation process. The Spectre simulator will pass operating point parameters to URI models that will iteratively age each device within the circuit. The process flow, shown in Figure 3.5, consists of:

1. Simulation of a circuit in pre-stress condition.
2. Transient simulation for a set number of circuit periods to iteratively accumulate the net aging of a device over a circuit period.
3. Extrapolation of aging for several periods to a determined lifetime.
4. Creation of an aged compact model parameter set.
5. Re-simulation of the circuit in post-stress condition with the aged parameter set.

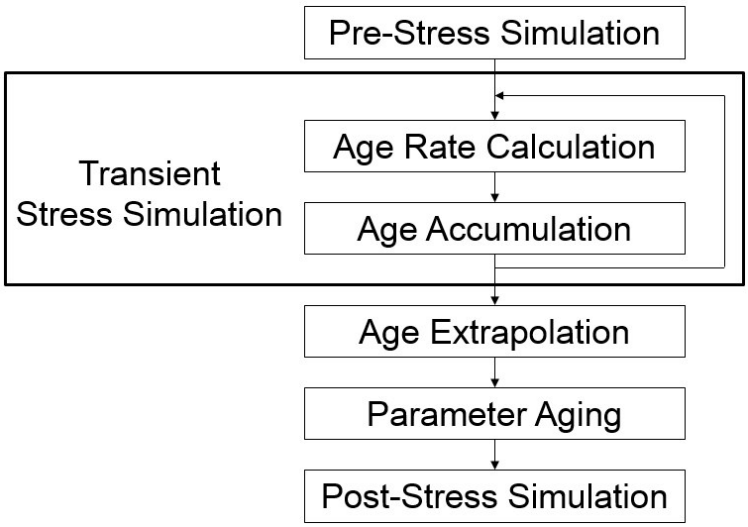


Figure 3.5: Simulation flow diagram for the aging process within Spectre.

Determining the age rate during the transient stress simulation is performed by summing the discretized degradation calculated using the formulated model at each time step during the circuit period. In performing this stress accumulation, the previously derived degradation equation takes the form

$$Age = \sum_{0}^{T} \left[\left(\sqrt{I_{avl} \cdot e^{-b\sqrt{\frac{1+I_E/I_1}{V_{bi}+V_{CB}}}} e^{-\frac{I_E}{I_0}}} \right)^{\frac{1}{n}} \cdot \Delta t \right] \tag{3.7}$$

After the transient simulation completes, the Age parameter can be linearly extrapolated to a full circuit lifetime, and the non-ideal base current compact model parameter can be aged by

$$I_{bn} = I_{bn,0} \left(1 + A_0 \frac{Age^n}{100} \right) \tag{3.8}$$

As this model is implemented external to the circuit simulation, this degradation model can easily be added to any bipolar compact model that has accurately modeled avalanche current.

3.4 Summary

We have formulated a physics-based degradation model for mixed-mode stress in SiGe HBTs. This model has been calibrated using both measured stress data and simulated TCAD stress data. Additionally, this degradation model has been implemented in the Spectre circuit simulator via the URI framework. The URI enables for the calculation of the device damage accumulated over a stress period and subsequent extrapolation to the full circuit lifetime. From this calculation, end-of-life compact model parameter sets are generated that enable the circuit designer to predict the end-of-life circuit performance. Additional work is still needed complete setup of the simulation environment, which is why no Spectre simulated stress data is presented here. Moving forward, we will investigate the modeling of additional degradation

mechanisms in addition to the mixed-mode damage mechanism in order to create a comprehensive hot carrier stress degradation model that will finally realize this "holy grail" of circuit simulation, efficient and accurate reliability simulation for full circuits.

CHAPTER 4

CONCLUSION

4.1 Contributions

The results presented in Chapter 2 on the effects of high-current stress in a first-generation SiGe HBT technology shows clear evidence of a new damage mechanism present at high-current density operation outside of the typical mixed-mode damage mechanism. Extensive measurement data covering a wide range of stress bias conditions at multiple temperatures is supported by TCAD simulation of a well-calibrated 2D model of the technology to show that Auger recombination is the culprit mechanism for hot carrier generation under such operating conditions. The results from this work are currently under review to be published in IEEE Transaction on Electron Devices [1] and are an extension of work presented at the IEEE International Semiconductor Device Research Symposium 2013 [18].

The results from Chapter 3 on the creation of a degradation compact model for mixed-mode damage in SiGe HBTs shows potential to be the foundation of a comprehensive hot carrier stress damage model for SiGe HBTs. The formulated model shows good fit to both measured stress data and TCAD simulated stress data, and the model has been set up for use in the Cadence Spectre circuit simulator.

4.2 Future Work

4.2.1 TCAD Modeling of Hot Carrier Effects

In order to more fully understand the effects of Auger hot carrier degradation, the TCAD stress damage framework developed in [8, 23] must be extended to support both the Auger hot carrier and annealing mechanisms in SiGe HBTs. We currently

have a simple model for Auger hot carrier degradation, but a more thorough approach to statistically characterize the degradation will be necessary to create an accurate and well calibrated model. The annealing process presents an additional challenge because our current efforts have been based on the assumption of a forward-reaction dominated process in the solution to the R-D equations. To properly model annealing behavior, finding full solutions to the R-D equations will be necessary.

4.2.2 Hot Carrier Degradation Model for Reliability-Aware Design

Once we are capable of running mixed-mode degradation simulations in Spectre, we will need to calibrate the simulation model to the measured stress data. Stress measurements on fundamental circuit elements such as current mirrors and simple switching elements is currently underway and will inform the validity and calibration of the compact degradation model. With a calibrated model, efficient investigation into the effects of device degradation on circuit operation may begin. The objective will be to explore circuit design techniques and novel architectures that either minimize individual device degradation or mitigate the effects of device degradation on overall circuit performance. Additionally, modeling of high-current and annealing stress behaviors will be necessary to create a complete compact degradation model.

REFERENCES

[1] B. Wier, U. Raghunathan, P. Chakraborty, H. Yasuda, P. Menz, and J. Cressler, "A comparison of field and current driven hot-carrier reliability in npn sige hbts," *Electron Devices, IEEE Transactions on*, vol. In Review, 2015.

[2] B. Heinemann, R. Barth, D. Bolze, J. Drews, G. Fischer, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, M. Lisker, S. Marschmeyer, H. Rucker, D. Schmidt, J. Schmidt, M. Schubert, B. Tillack, C. Wipf, D. Wolansky, and Y. Yamamoto, "Sige hbt technology with ft/fmax of 300ghz/500ghz and 2.0 ps cml gate delay," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, pp. 30.5.1–30.5.4, Dec 2010.

[3] P. Chakraborty, A. Cardoso, B. Wier, A. Omprakash, J. Cressler, M. Kaynak, and B. Tillack, "A 0.8 thz f_max sige hbt operating at 4.3 k," *Electron Device Letters, IEEE*, vol. 35, pp. 151–153, Feb 2014.

[4] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistor*. Boston, MA: Artech House, Inc., 2003.

[5] G. Zhang, J. Cressler, G. Niu, and A. Joseph, "A new "mixed-mode" base current degradation mechanism in bipolar transistors," in *Bipolar/BiCMOS Circuits and Technology Meeting, 2002. Proceedings of the 2002*, pp. 32–35, 2002.

[6] P. Cheng, C. Zhu, A. Appaswamy, and J. Cressler, "A new current-sweep method for assessing the mixed-mode damage spectrum of sige hbts," *Device and Materials Reliability, IEEE Transactions on*, vol. 7, pp. 479–487, Sept 2007.

[7] D. J. DiMaria and J. W. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *Journal of Applied Physics*, vol. 65, no. 6, pp. 2342–2356, 1989.

[8] K. Moen, P. Chakraborty, U. Raghunathan, J. Cressler, and H. Yasuda, "Predictive physics-based tcad modeling of the mixed-mode degradation mechanism in sige hbts," *Electron Devices, IEEE Transactions on*, vol. 59, pp. 2895–2901, Nov 2012.

[9] S. Tam, P.-K. Ko, and C. Hu, "Lucky-electron model of channel hot-electron injection in mosfet's," *Electron Devices, IEEE Transactions on*, vol. 31, pp. 1116–1125, Sep 1984.

[10] K. Hasnat, C.-F. Yeap, S. Jallepalli, W.-K. Shih, S. Hareland, J. Agostinelli, V.M., J. Tasch, A.F., and C. Maziar, "A pseudo-lucky electron model for simulation of electron gate current in submicron nmosfet's," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 1264–1273, Aug 1996.

[11] Synopsys, Inc., *Sentaurus Device User Guide*, 2012.

[12] K. O. Jeppson and C. M. Svensson, "Negative bias stress of mos devices at high electric fields and degradation of mnos devices," *Journal of Applied Physics*, vol. 48, no. 5, pp. 2004–2014, 1977.

[13] C. Zhu, Q. Liang, R. Al-Huq, J. Cressler, Y. Lu, T. Chen, A. Joseph, and G. Niu, "Damage mechanisms in impact-ionization-induced mixed-mode reliability degradation of sige hbts," *Device and Materials Reliability, IEEE Transactions on*, vol. 5, pp. 142–149, March 2005.

[14] R. A. Wachnik, T. J. Bucelot, and G. P. Li, "Degradation of bipolar transistors under high current stress at 300 k," *Journal of Applied Physics*, vol. 63, no. 9, pp. 4734–4740, 1988.

[15] M. Carroll, A. Neugroschel, and R.-Y. Sah, "Degradation of silicon bipolar junction transistors at high forward current densities," *Electron Devices, IEEE Transactions on*, vol. 44, pp. 110–117, Jan 1997.

[16] J.-S. Rieh, K. Watson, F. Guarin, Z. Yang, P.-C. Wang, A. Joseph, G. Freeman, and S. Subbanna, "Reliability of high-speed sige heterojunction bipolar transistors under very high forward current density," *Device and Materials Reliability, IEEE Transactions on*, vol. 3, pp. 31–38, June 2003.

[17] C. Tsai, M. Chen, S. Ku, and T. Wang, "Auger recombination-enhanced hot carrier degradation in nmosfets with a forward substrate bias," *Electron Devices, IEEE Transactions on*, vol. 50, pp. 1022–1026, April 2003.

[18] B. Wier, U. Raghunathan, P. Chakraborty, J. Cressler, H. Yasuda, and P. Menz, "Base current degradation mechanisms in npn sige hbts subjected to high current stress," in *Semiconductor Device Research Symposium (ISDRS), 2013 International*, pp. 1–2, Dec 2013.

[19] M. Govoni, I. Marri, and S. Ossicini, "Auger recombination in si and gaas semiconductors: *Ab initio* results," *Phys. Rev. B*, vol. 84, p. 075215, Aug 2011.

[20] S. Rauch, G. La Rosa, and F. J. Guarin, "Role of e-e scattering in the enhancement of channel hot carrier degradation of deep-submicron nmosfets at high vgs conditions," *Device and Materials Reliability, IEEE Transactions on*, vol. 1, pp. 113–119, Jun 2001.

[21] L. Huldt, N. G. Nilsson, and K. G. Svantesson, "The temperature dependence of bandtoband auger recombination in silicon," *Applied Physics Letters*, vol. 35, no. 10, pp. 776–777, 1979.

[22] P. Jonsson, H. Bleichner, M. Isberg, and E. Nordlander, "The ambipolar auger coefficient: Measured temperature dependence in electron irradiated and highly

injected n-type silicon," *Journal of Applied Physics*, vol. 81, no. 5, pp. 2256–2262, 1997.

[23] U. Raghunathan, P. Chakraborty, T. Gibremariam, B. Wier, H. Yasuda, P. Menz, and J. Cressler, "Bias and temperature dependent accumulated stress modeling of mixed-mode damage in sige hbts," *Electron Devices, IEEE Transactions on*, vol. In Review, 2015.

[24] M. Oakley, U. Raghunathan, B. Wier, P. Chakraborty, and J. Cressler, "Large-signal reliability analysis of sige hbt cascode driver amplifiers," *Electron Devices, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[25] C. Hu, "Ic reliability simulation," *Solid-State Circuits, IEEE Journal of*, vol. 27, pp. 241–246, Mar 1992.

[26] F. Marc, B. Mongellaz, C. Bestory, H. Levi, and Y. Danto, "Improvement of aging simulation of electronic circuits using behavioral modeling," *Device and Materials Reliability, IEEE Transactions on*, vol. 6, pp. 228–234, June 2006.

[27] B. Ardouin, J.-Y. Dupuy, J. Godin, V. Nodjiadjim, M. Riet, F. Marc, G. Kone, S. Ghosh, B. Grandchamp, and C. Maneux, "Advancements on reliability-aware analog circuit design," in *Solid-State Device Research Conference (ESSDERC), 2012 Proceedings of the European*, pp. 62–68, Sept 2012.

[28] P. Cheng, C. Grens, and J. Cressler, "Reliability of sige hbts for power amplifiers – part ii: Underlying physics and damage modeling," *Device and Materials Reliability, IEEE Transactions on*, vol. 9, pp. 440–448, Sept 2009.

[29] P. Cheng, A. Appaswamy, M. Bellini, and J. Cressler, "Probing hot carrier phenomena in npn and pnp sige hbts," in *Silicon Monolithic Integrated Circuits in RF Systems, 2008. SiRF 2008. IEEE Topical Meeting on*, pp. 54–57, Jan 2008.

[30] J. Kirk, C.T., "A theory of transistor cutoff frequency (ft) falloff at high current densities," *Electron Devices, IRE Transactions on*, vol. 9, pp. 164–174, March 1962.

[31] Cadence Design Systems, Inc., *Virtuoso® Unified Reliability Interface Reference*, 2014.